Syllabus

EE 498 VHDL (VHSIC Hardware Description Language)  
Fall, 2014

Engineering/Physics Department

<table>
<thead>
<tr>
<th>Section</th>
<th>EE251</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instructor</td>
<td>Dr. David R. Carey</td>
</tr>
<tr>
<td>email</td>
<td><a href="mailto:david.carey@wilkes.edu">david.carey@wilkes.edu</a></td>
</tr>
<tr>
<td>phone</td>
<td>570-408-4807</td>
</tr>
<tr>
<td>office</td>
<td>SLC-221</td>
</tr>
</tbody>
</table>

Office Hours: As posted on office door or by appointment.

Lecture and Location:
W 16:00-20:45 SLC-223

Prerequisites: Graduate Standing

Textbook: Provided in Class and online

Objectives: Functional verification is one of the most complex and expensive tasks in the current system-on-chip (SOC) design methodology. Various studies have shown that the verification consumes more than 70% of the total design cost (time). The goal of this course is to develop a comprehensive understanding of the technologies behind hardware verification. The students will develop an appreciation of the existing capabilities and limitations of various hardware modeling and verification methods. The course will cover the basics of modeling and simulation using VHDL/Verilog, and hardware verification using formal techniques such as symbolic simulation, model checking, theorem proving, satisfiability solving, and equivalence checking. The lectures will also cover case studies of verifying complex systems including verification of Intel microprocessors. Three hours of lecture per week.

Lectures: You are responsible for all material covered in the textbook and in lecture, including any announcements made or special handouts distributed in lecture. If you must be absent during a given lecture, check with a friend to make sure you know what was covered.

Reading Assignments: Students are expected to read the relevant text book chapters and all handouts by the assigned class period.

Computer Use: Students are expected to use computers to do analyses, to prepare reports, and to conduct out-of-class assignments. Computers will be used to analyze data, prepare engineering graphs for reports, and perform analytic studies. Knowledge of word-processing, spreadsheet, and analysis software (i.e., Quartus, Word, Excel, Matlab, etc.) is required.
**Syllabus**

EE 498 VHDL (VHSIC Hardware Description Language)  
Fall, 2014

**Homework:** The weekly assignments represent by far the most important element of the course, and where you will learn the most. I encourage you to work on them in groups if you like; the assignments will occasionally be difficult and may require more than one head! However, be convinced in the depths of your soul that letting others do the work for you will lead to disaster at test time. A good technique for many students is to try the assignment individually, then to get together with a friend or in a group for the tough ones. Many years of experience have shown that students who do not work the assignments thoroughly do not really understand the material and perform poorly at test time. Reading the text is never sufficient! You are expected to do your homework assignments by their due dates and have them available in class.

You may receive help on these or even work with another student. However, if you do this, please indicate the degree of your own involvement. If you simply submit a copy of another student's work, explain your own role in doing the assignment, which should not be limited to just operating the copier. The degree to which students participate in doing homework will be subjectively judged and may influence the final grade by up to a point in either direction in borderline cases, as well as affecting the subjective "class participation" part of the grade. The intent here is to allow any degree of cooperation and help on the homework.

**Grading:** You are welcome to discuss the assignments with other students or with the instructor after you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas.

If you miss an assignment for a valid, verified emergency, see your instructor. *Letter grades will not be based on a curve but rather on the following fixed scale:*

\[
93-100 = 4.0, 88-92 = 3.5, 83-87 = 3.0, 77-82 = 2.5, 70-76 = 2.0, 65-69 = 1.5, 60-64 = 1.0, \text{below 60} = 0.0
\]

The advantage of the fixed scale is that you are not competing with other students to “get ahead of the curve.” Everyone who works hard can do well in the class. It is possible that the entire class can receive A’s (all scores would be 93% or better). Those who do not do the work will score accordingly.

<table>
<thead>
<tr>
<th>Homework</th>
<th>10%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test 1</td>
<td>15%</td>
</tr>
<tr>
<td>Test 2</td>
<td>15%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>30%</td>
</tr>
<tr>
<td>Project</td>
<td>20%</td>
</tr>
<tr>
<td>Class Participation</td>
<td>10%</td>
</tr>
</tbody>
</table>

**How to succeed in this course:**

1. It is expected that a successful student will attend all classes and submit all homework. Do not expect a good grade if you are not prepared to work at least this much.
2. Read the assigned text before coming to lecture. The importance of this cannot be overemphasized.
3. Work as many problems as possible on a weekly basis; the assigned ones represent the minimum recommended. Do these on your own, if possible; then work with other students to solve the problems.
4. Keep up on a regular basis; cramming doesn’t work.
5. **No late homework will be accepted.**
6. Plagiarized homework from another student will result in an automatic zero for all parties involved.
7. **No make-up exams will be given.**
8. **Class attendance is mandatory.**
Course Outline: Tentative course outline is shown below.

1. Introduction to Hardware Modeling and Verification
   - **Reading:**
   - *The Ten Commandments of Excellent Design* by Peter Chambers

2. Hardware Modeling using Verilog
   - **Reading:**
   - *Handbook on Verilog HDL* by Daniel Hyde

3. Hardware Modeling using VHDL
   - **Reading:**
   - *The Designer's Guide to VHDL* by Peter J. Ashenden

4. Test #1

5. Hardware Simulation
   - **Reading:**
   - *Architecture description languages for programmable embedded systems*
   - *A Universal Technique for Fast and Flexible Instruction Set Architecture Simulation*
   - *Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation*
   - *An Efficient Retargetable Framework for Instruction-Set Simulation*
   - *Memory Access Optimizations in Instruction-Set Simulators*

6. Binary Decision Diagrams
   - **Reading:**
   - *Graph-Based Algorithms for Boolean Function Manipulation* by Randal E. Bryant

7. Test #2

8. Model Checking
   - **Reading:**
   - *Model Checking* by Edmund Clarke, Orna Grumberg, and D. Long.

9. Symbolic Simulation
10. Equivalence Checking
11. Satisfiability Solvers
12. Theorem Proving
13. Manufacturing Testing
   - **Reading:**
   - *Design for Test Methodology Case Study for Motorola C-5e DCP Using the Cadence Incisive Accelerator/Emulator* by Justin Hernandez